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DRAM CELL WITH SELF-ALIGNED CONTACT AND METHOD OF FABRICATING SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to dynamic random access memories (DRAMs) and, in particular, to a DRAM cell structure with a self-aligned contact which reduces cell size while maintaining high cell capacitance.

2. Discussion of the Relevant Art

Reduction in the size of a DRAM cell utilizing a stacked gate cell capacitor is limited by the design rule for the transistor's contact-to-gate spacing. This is because the layout must account for mask misalignment in forming the contact to the gate utilizing conventional lithographic processing techniques. Also, as DRAM cell size becomes smaller, the cell capacitance becomes unacceptably small. A small cell capacitance reduces the sense amplifier signal, thereby deteriorating DRAM robustness and worsening the soft-error performance problem.

A variety of DRAM cell innovations for increasing the capacitance while keeping the cell area small have been reported in DRAM cell literature. A good review of different approaches can be found in Chapters 4 and 6, "Semiconductor Memories - A Handbook of Design, Manufacture, and Applications," John Wiley & Sons, 1991, by Betty Prince.

Figs. 1a and 1b illustrate a prior art DRAM cell 10, commonly called a Stacked Capacitor Cell (STC). Fig. 1a shows a cross-section of the STC, while Fig. 1b shows the corresponding layout.

In accordance with the process flow for fabricating the STC structure, the device active area 12 and the transistor gate 14 (poly1) are defined in the conventional manner. After deposition of the interlayer dielectric 16, a contact mask is used to etch contact trench 18. Bottom poly (poly2) is then deposited and patterned to form the bottom plate 20 of the capacitor which is connected to the transistor source 22 via the contact trench 18. Capacitor dielectric 24 is then grown or deposited on the poly2 bottom plate 20. The top poly (poly3) is then deposited and patterned to provide the poly3 top plate 26 of the capacitor, completing the basic STC structure. Other layers of the STC structure not relevant to the present discussion are not shown.

The area of the interpoly dielectric 24 between poly2 bottom plate 20 and poly3 top plate 26 determines the STC's coupling capacitance. Referring to the Fig. 1a cross-section, it should be noted that typical diameter of the contact trench 18 is 0.5μm, whereas the thickness is about 5KÅ. The CVD poly2 completely fills the contact trench 18 and, thus, the capacitor area basically lies above the contact, not in the contact. Reducing the poly2 thickness would allow the capacitor to be formed inside the contact trench 18, but it also reduces the sidewall capacitor area. A relatively thicker poly2 also does not produce a vertical profile inside the contact trench 18, and the capacitance may not be very reproducible. It should be noted that, in the above-described technique and it's variations, the contact trench 18 must be placed sufficiently far away from the transistor gate 14 to allow for lithography misalignment. This increases the cell size.

Figs. 2a and 2b show an improvement over the STC structure shown in Figs. 1a and 1b. This improved DRAM cell structure 50 results in the cell capacitor being formed inside the contact trench, thus resulting in a higher cell capacitance. Fig. 2a shows the cross-section of the DRAM cell; the corresponding layout is shown in Fig. 2b.

A variety of process sequences can be utilized in fabricating the structure shown in Figs. 2a and 2b. There can even be some variations in the layer deposition and patterning sequence. In accordance with one process flow, device active area 52 and transistor gate 54 (poly 1) are defined in the conventional manner. After deposition of the interlayer dielectric 56, an extra layer of thick poly 58 (poly2) is deposited. The thickness of poly 58 typically can be in the 2KÅ to 10KÅ range. A contact mask is then used to pattern and etch contact trench 60 by first etching the thick poly2 58 and then the dielectric 56. A thin poly layer (poly3), in the range of 200Å to 1.5KÅ thick, is then deposited and patterned to form the bottom plate of the capacitor. The bottom plate, constituted now by poly2 58 and poly3 62, connects to the transistor source 63 via contact trench 60. Note that poly2 58 and poly3 62 are patterned and etched together, thus reducing the number of masking steps. This process also avoids extra overlap required on both sides of the lower poly2 58 by upper poly3 62, thereby reducing the cell size. Capacitor dielectric 64 is then grown or deposited on the poly3 plate 62. The top poly (poly4) is then deposited and patterned to form upper plate 66, completing the basic structure of the DRAM cell. Other layers of the device

structure not relevant to the present discussion are not shown.

The area of the interpoly dielectric 64 between the lower poly2/3 plate and the upper poly4 plate determines it's capacitance. It should be noted that for a given technology and typical diameter of the contacts, the poly3 thickness is chosen such that the contact trench 60 is not filled after the capacitor dielectric growth or deposition. The capacitor thus can extend into the contacts.

A variation of the above structure can be obtained by patterning the poly2 58 before depositing poly3 by using the mask represented by layer 62 in Fig. 2b or it's oversized mask. This may give a more uniform capacitor dielectric growth by eliminating the poly2\poly3 interface in the sidewalls, but increases the number of masks.

Neither of the above-described structures attempts to reduce the DRAM cell size by utilizing a self-aligned contact.

SUMMARY OF THE INVENTION

The present invention provides a technique for reducing DRAM cell area by eliminating the contact-to-gate spacing requirement while increasing the capacitor area by designing the capacitor to extend inside the contact, without sacrificing the sidewall capacitance. The new structure uses a self-aligned contact where the contact can overlap the gate region in the layout.

Other features and advantages of the present invention will become apparent and be appreciated by reference to the following detailed description which should be considered in conjunction with the accompanying drawings.

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DESCRIPTION OF THE DRAWINGS

Figs. 1a and 1b show the cross-section and layout, respectively, of a prior art DRAM Stacked Capacitor Cell.

Figs. 2a and 2b show the cross-section and layout, respectively, of another prior art DRAM cell.

Figs. 3a and 3b show the cross-section and layout, respectively, of a DRAM cell with a self-aligned contact formed in accordance with the present invention.

Fig. 4 is a schematic representation of the DRAM cell shown in Figs. 3a and 3b and illustrating the use of the poly layers.

DETAILED DESCRIPTION OF THE INVENTION

The following detailed description is of the best modes presently contemplated by the inventor for practicing the invention. It should be understood that the description of these preferred embodiments is merely illustrative and should not be taken as limiting of the claimed invention.

Figs. 3a and 3b show a DRAM cell 100 that incorporates a self-aligned contact, thereby allowing the cell size to be reduced. Fig. 3a shows a cross-section of the DRAM cell 100; the corresponding layout of the cell 100 is shown in Fig. 3b.

A variety of fabrication sequences can be used to provide the cell 100 shown in Figs. 3a and 3b. One embodiment of a process flow to achieve the self-aligned structure of cell 100 is discussed below.

First, active area 102 is defined in the conventional manner. The transistor gate 104 is patterned and etched after deposition of gate poly (poly1), a silicide layer 106 (e.g., Tungsten

silicide), and a dielectric layer 108 (e.g., TEOS oxide), all in accordance with conventional techniques. Next, dielectric deposition and etching steps are performed to produce sidewall spacers 110; the dielectric may be LTO or other conventional dielectric material suitable for this purpose. A layer of dielectric 112, such as LTO, is then deposited; the thickness of dielectric 112 is such that it can be etched reproducibly (later) without etching too much into dielectric 108. A layer of thick poly 114 (poly2) is then deposited. The thickness of this poly2 typically can be in the 2KÅ to 10KÅ range. A contact mask is used to pattern and etch contact trench 116, by first etching the poly2 114 and then the dielectric 112. A thin poly layer (poly3), in the range of 200Å to 1.5KÅ thick, is then deposited and patterned to form the poly3 plate 118 of the capacitor, which connects the transistor source 120 to bottom capacitor plate constituted now by poly2 114 and poly3 118. It should be noted that the contact etch should clear the gate dielectric in the source region 120 reproducibly while ensuring that dielectric 108 is not etched significantly to allow a high capacitance or shorts between poly3 118 and the transistor gate 104/106. Capacitor dielectric 122 is then grown or deposited on poly3 118. The top poly (poly4) is then deposited and patterned to provide the upper capacitor plate 124, completing the basic structure of the DRAM cell 100. Other layers of the final device structure not relevant to present discussion are not shown. The area of the interpoly dielectric 122 between poly2/3 lower plate 114/118 and poly4 upper plate 124 determines it's capacitance.

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It should be noted that, for a given technology, the cell size for this implementation can be smaller than that shown in either the Fig. 1a/1b or the Fig. 2a/2b structures. At the same time, the contact size can be larger than in these prior art cells. This is because there is no design rule for contact to gate spacing, and the poly3 118 contacts the source 120 in a "self-aligned" manner, i.e., regardless of the location of the contact edge on top of the poly gate 104/106, the physical poly3-to-source interface on the gate side is unchanged.

Fig. 4 provides a schematic representation of the cell 100 described above in conjunction with Figs. 3a and 3b illustrating the various interconnect layers forming the cell.

Although the present invention has been described in terms of the presently preferred embodiments, it is to be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications that fall within the true spirit and scope of the invention.

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